ABSTRACT OF THE DISCLOSURE

A semiconductor memory device is provided as well as a method for operating the semiconductor memory device. The memory device includes a NOR array of memory cells and a NAND array of memory cells configured on the same monolithic semiconductor substrate. Each cell of the NOR array involves a single transistor, similar to each cell of the NAND array. The memory device is, therefore, an integrated circuit that includes not only the NOR and NAND arrays, but also the row and column decoders corresponding to each array. Furthermore, the integrated circuit includes the interface circuitry needed to transfer information as pages into and from the NAND array. The corresponding interface or controller is implemented on the same monolithic substrate as both the NAND array and the NOR array. Addresses targeted for the NOR array are sent as fully memory-mapped data into the NOR array, whereas addresses targeted for the NAND array are sent through the controller integrated within the semiconductor memory device. The single transistor cell of both the NAND array and NOR array preferably involves a flash EEPROM-type transistor that implements a floating gate dielectrically spaced between a control gate and the semiconductor substrate.